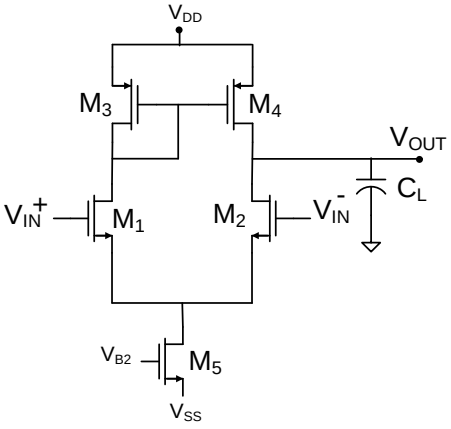
EE 435 Name_____
Exam 1
Spring 2023
Due Friday March 24 at 5:00 p.m. – Upload as a .pdf file in Canvas
Instructions: The points allocated to each problem are as indicated. Note that the first is weighted more heavily than the rest of the problems. On those problems that need technology parameters that are not given in the problem, assume you are working in a 0.5µm CMOS process with process parameters $\mu_n C_{OX} = 100\mu A/V^2$, $\mu_p C_{OX} = 33\mu A/V^2$, $V_{Tn} = 0.75V$, $V_{Tp} = -0.75V$, $C_{OX} = = 2fF/\mu^2$, $\lambda = 0.01v^{-1}$, $\gamma = 0$, and $A_{VT0} = 20mV\bullet\mu m$ for both n-channel and p-channel devices.

As a take-home exam, all work on this exam must be done individually. There should be no collaboration with anyone except for the course instructor, R. Geiger. (That means absolutely no use of online sources such as Chegg or other online services) If there are any questions, it might be easiest to address them by email to the course instructor. An immediate response cannot be promised but I will check my email periodically throughout the duration of this exam.

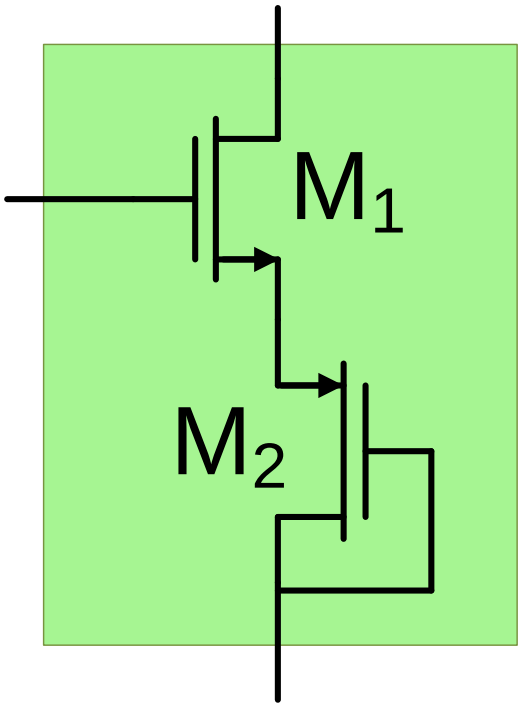
Problem 1 (20 points) The operational amplifier has been designed with $|V_{EB}| =$ 200mV for all transistors with a total power dissipation of 5mW when biased with a symmetric 2.5V supply (i.e. $V_{DD}=2.5V$ and $V_{SS}=-2.5V$). The load capacitor is $C_L=10pF$ and the length of all transistors are 4µm.

a) Determine the GB of the op amp
b) What is the W/L ratio of M_3?
c) Determine an acceptable value for V_{B2}
d) Express the dc gain in terms of the small-signal model parameters of the devices.
e) Give a numerical value for the dc gain of this op amp.
f) What is the 3dB bandwidth?
g) What is the slew rate of the op amp?
h) What is the input-referred offset voltage due to local random variations (give the standard deviation of the offset voltage)
i) If connected in a unity gain feedback configuration, what is the 3dB bandwidth
j) What is the phase margin if connected in a unity gain feedback configuration
k) What is the output signal swing if the common-mode input voltage is 0.5V.



Problem 2 (10 points) Consider the following circuit as a quarter circuit.

a) Give the circuit schematic of a differential input – differential output operational amplifier derived from this quarter circuit using a tail current bias. Assume a load capacitance of C_L on both of the outputs of this operational amplifier (Show where the CMFB is connected but do not design the CMFB circuit)
b) Give an expression for the dc voltage gain of the operational amplifier in terms of the small-signal model parameters.
c) Give an expression for the GB of the operational amplifier

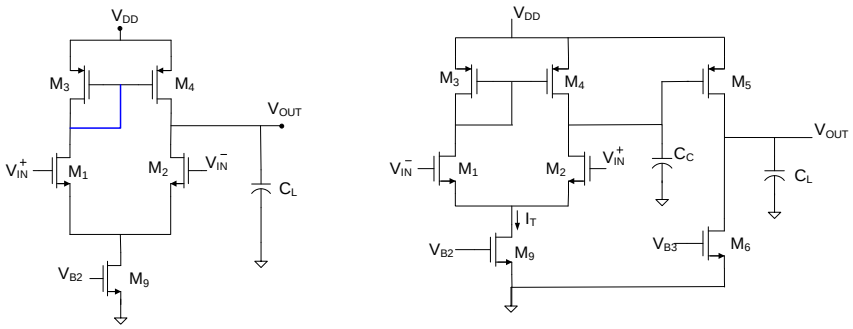


Problem 3 (10 points) Consider the two operational amplifiers shown below denoted as the 5T and the 7T op amps respectively. Assume the load capacitance is fixed and the 7T op amp is compensated with the dominant pole on the output node of the first stage with the compensation capacitor C_C with a pole spread of $3\beta A_0$ where A_0 is the dc voltage gain of the 7T op amp.

a) Obtain an expression for the GB of the two amplifiers in terms of the small-signal model parameters

b) Obtain an expression of the GB of the two amplifiers in terms of the practical parameters {V_{EB1}, V_{EB5}, P, and θ} where P is the total power dissipation and for the 7T amplifier, θ is the fraction of the total power dissipated in the second stage.

c) If both are connected in a unity-gain feedback configuration to serve as a buffer (i.e. β=1), compare the GB power efficiency (GB/P) of the two amplifiers. When making this comparison, pick θ to optimize the GB power efficiency of the 7T feedback amplifier.

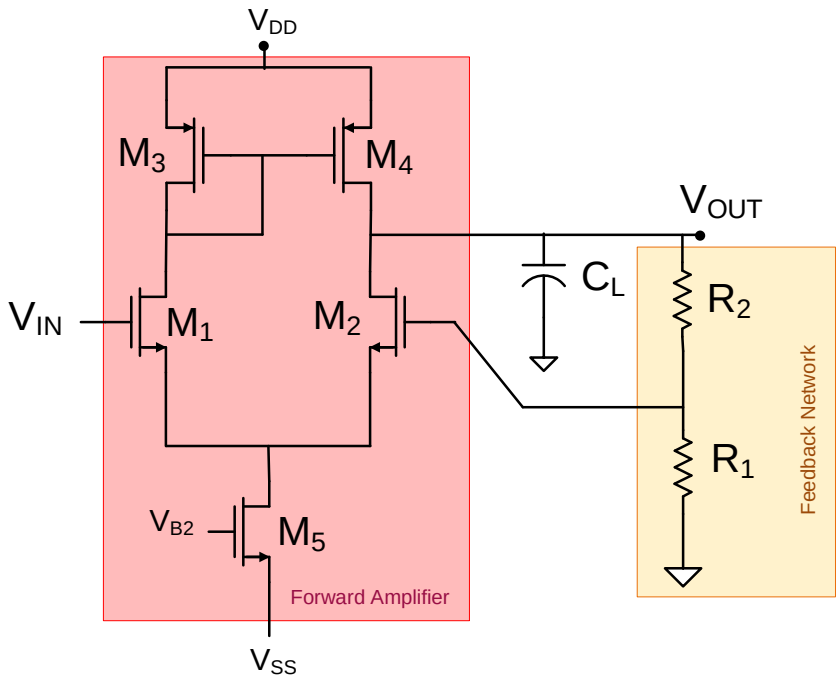


Problem 4 (10 points) It was shown that if a second-order all-pole amplifier with gain $A(s)=\dfrac{A_0}{\left(\dfrac{s}{p}+1\right)\left(\dfrac{s}{kp}+1\right)}$ (where k is the open loop pole spread, and p and A_0 are both positive) is used in a standard feedback amplifier with closed loop gain $A_{FB}(s)=\dfrac{A}{1+A\beta}$, the open loop amplifier must be compensated to have an pole spread of approximately $4\beta A_0$ to have a closed-loop pole Q of ½. Consider now a modification of the A(s) amplifier so that the open-loop pole is moved into the RHP resulting in the open-loop gain expression $A(s)=\dfrac{-A_0}{\left(\dfrac{s}{-p}+1\right)\left(\dfrac{s}{kp}+1\right)}$ where now k is the ratio of the high frequency pole to the magnitude of the low frequency pole.

a) Analytically determine the value of k that must be achieved with compensation to obtain a closed-loop pole Q of 1/2.
b) Is the modified open-loop op amp stable?
c) What will be the phase margin of the closed-loop amplifier (using the original op amp) if the closed-loop pole has Q=1/2?
d) What will be the phase margin of the closed-loop amplifier using the modified op amp if the closed-loop pole has Q=1/2?

Problem 5 (10 points) Consider again the 5T op amp with the same specifications as in Problem 1 that drives a feedback network (β network) shown below where R_2=4KΩ and R_1=1KΩ.

a) What is β for this feedback amplifier
b) If the op amp is ideal, what will be the dc closed-loop gain?
c) What is the actual dc gain of the closed-loop feedback amplifier?
d) What is the loop gain if the loading by the β network is neglected
e) What is the loop gain if the loading of the β network is included?
f) Quantitatively compare the effective open loop gain of the op amp when connected in this feedback configuration with that obtained when the loading of the β network is neglected?



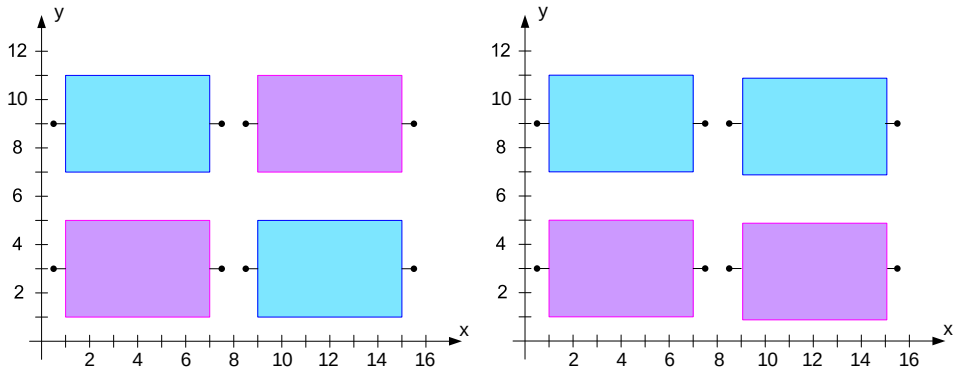
Problem 6 (10 points) A designer asked the layout technician to layout a differential pair using a common-centroid layout with two devices connected in parallel to form each transistor. The differential pair was used in the single-stage op amp shown below. The desired layout is shown on the left in the figure below with blue corresponding to the channel of transistor M_1 and purple corresponding to the channel transistor M_2. The drain and sources are on the left and right sides of the corresponding rectangles. But through a communication error, the actual layout that was obtained was that on the right. The dimensions on the axis are in µm. Assume $\mu C_{OX}=100\mu AV^{-2}$ and the threshold voltage at x=0 and y=0 was the nominal value of 0.75V.

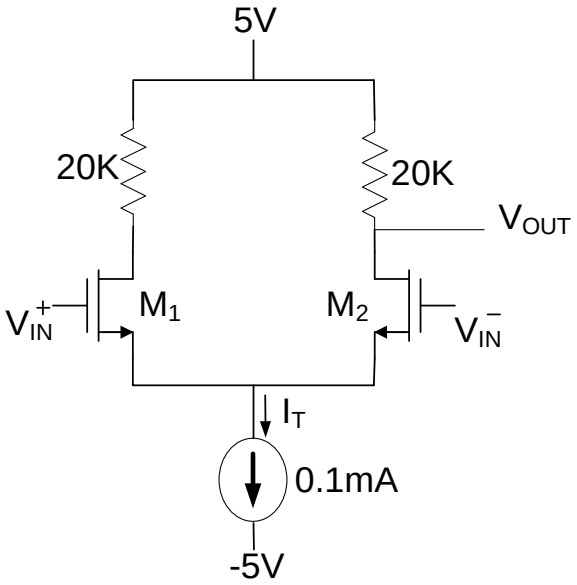
a) Determine the actual threshold voltage that would have been obtained for M_1 and M_2 (using the desired layout on the left) if there is a positive gradient at +45 degrees relative to the x-axis of magnitude 4mV/µm.

b) Determine the actual threshold voltage that will be achieved if the layout on the right were used.

c) Determine the input offset voltage due to the gradient that would have been achieved if the common-centroid layout on the left were used and that which will be obtained if the undesired layout on the right were used.

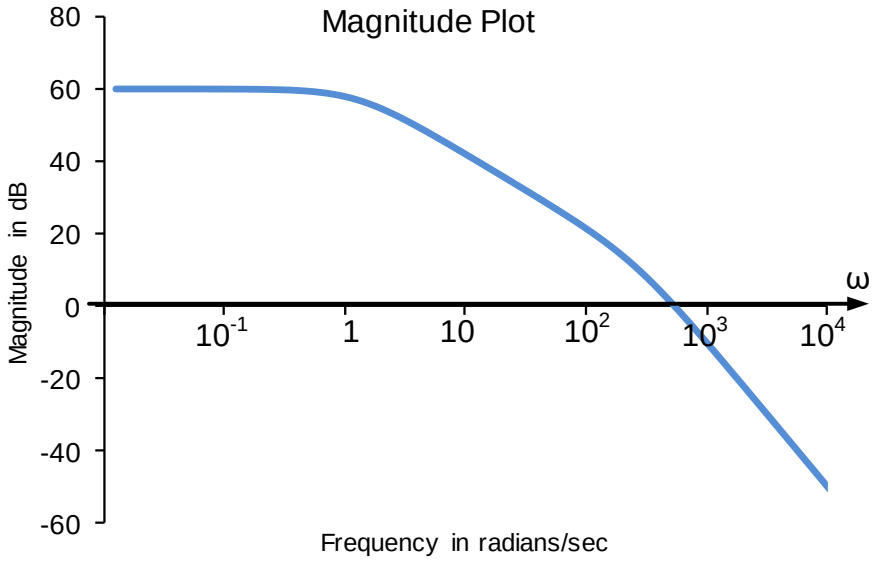
d) Repeat parts a)-c) if the gradient magnitude is the same but the direction is at 0^o relative to the x axis.

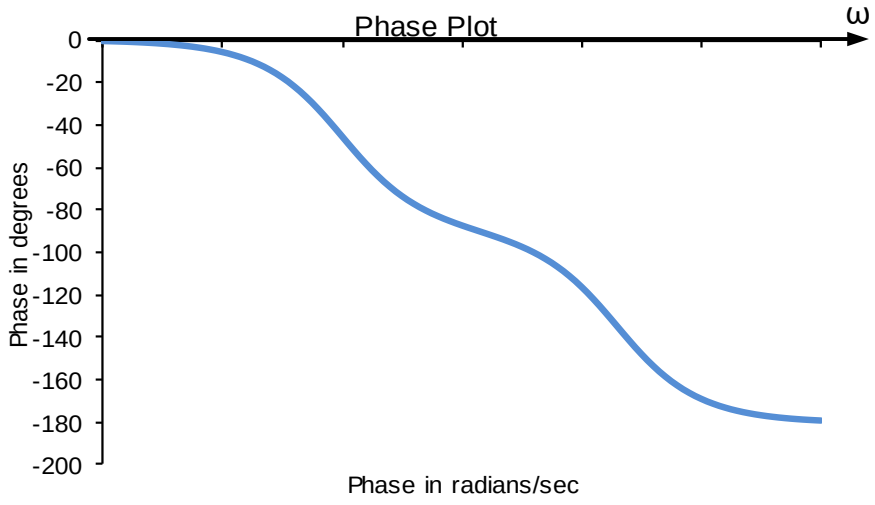




Problem 7 (10 points) The magnitude and phase plots of a differential input, single-ended output all-pole operational amplifier are shown below.

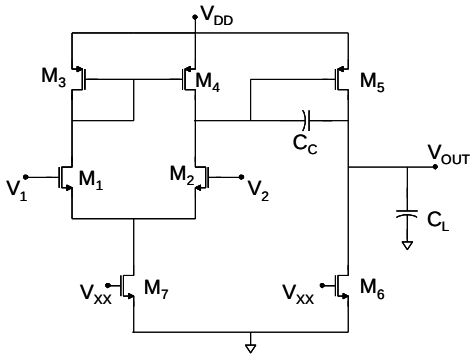
a) Determine the phase margin if this is used in a feedback amplifier with a feedback factor of β=0.05
b) Is the feedback amplifier stable? Why?
c) What is the maximum value of β that can be used if the amplifier is to have a 75° phase margin?
d) If β = 0.05, what is the ideal dc closed loop gain if configured as a basic noninverting feedback amplifier and what is the percent closed-loop gain error due to the finite dc gain limitations of the op amp?
e) How many poles does this amplifier have?





Problem 8 (10 points) A two-stage operational amplifier is shown. Assume V_{DD}=5V. Assume that the total power dissipation is 5mW and the power in the second stage is 5 times the power in the first stage.

a) Size M_7 and determine V_{XX} so that V_{EB7} is 150mV.
b) Size M_6 (assume V_{XX} is as determined in part a))
c) With the constraints given in the problem and in steps a)-b), identify the number of degrees of freedom remaining in the design of this circuit. With these constraints, complete the design leaving one degree of freedom to determine C_C.
d) Determine C_C in your design so that the magnitude response is maximally flat if connected in a noninverting feedback configuration with β=0.2. Assume C_L=500fF and assume the β network does not load the amplifier.
e) Determine the GB of your design
f) Determine the common-mode input range and the output range of your amplifier.



Problem 9 (10 points) A basic charge-redistribution successive-approximation ADC is shown below. In this structure, the Boolean inputs are adjusted until the voltage on the "+" terminal of the comparator is approximately 0. This condition is detected by the comparator. Consider a modification of this structure where the "-" terminal is connected to a dc voltage of value V_{XX} and the successive-approximation process is again used to force the voltage on the "+" terminal to be equal to V_{XX}. Give an expression for the Boolean output voltage and interpret the results.